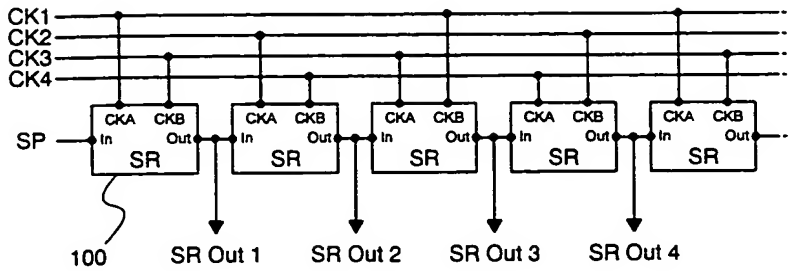
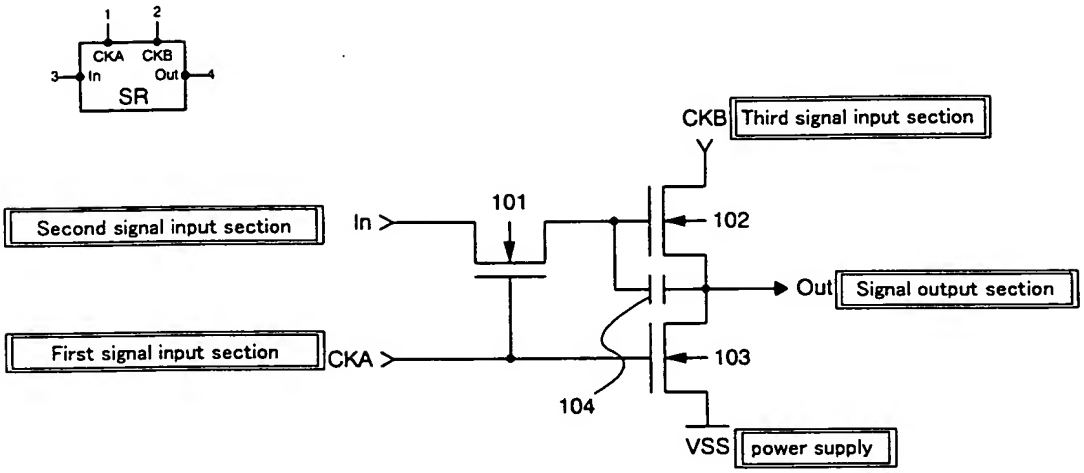
Fig. 1A



CK1 : First clock signal
CK2 : Second clock signal
CK3 : Third clock signal
CK4 : Fourth clock signal
SP : Start pulse

Fig. 1B



101 : First transistor
102 : Second transistor
103 : Third transistor
104 : Capacitor

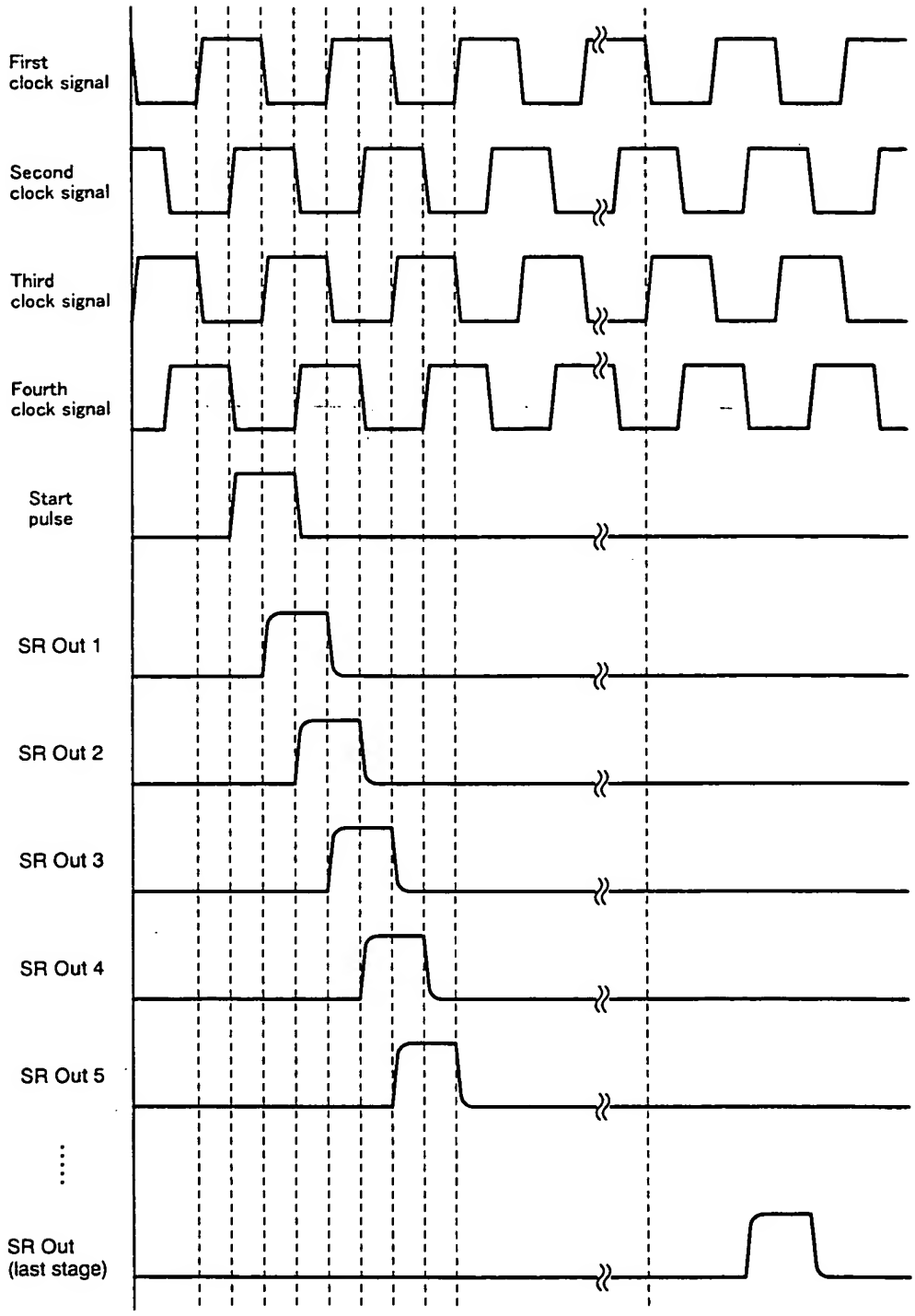
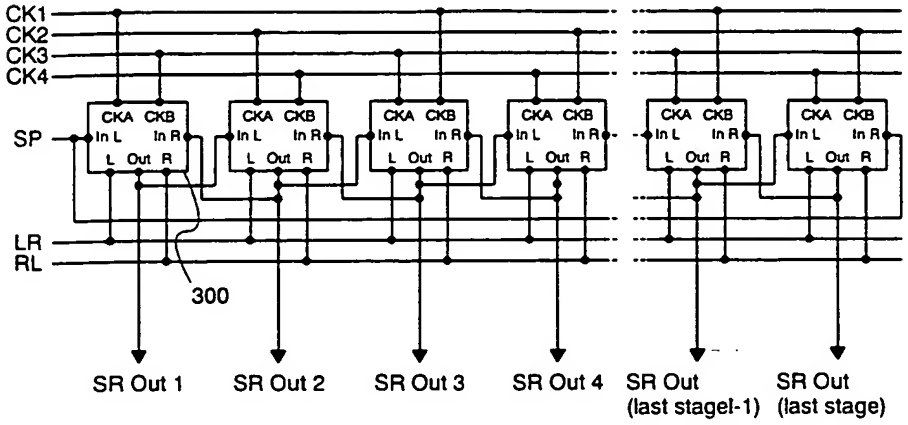

First clock signal
Second clock signal
Third clock signal
Fourth clock signal
Start pulse
SR Out 1
SR Out 2
SR Out 3
SR Out 4
SR Out 5
SR Out (last stage)

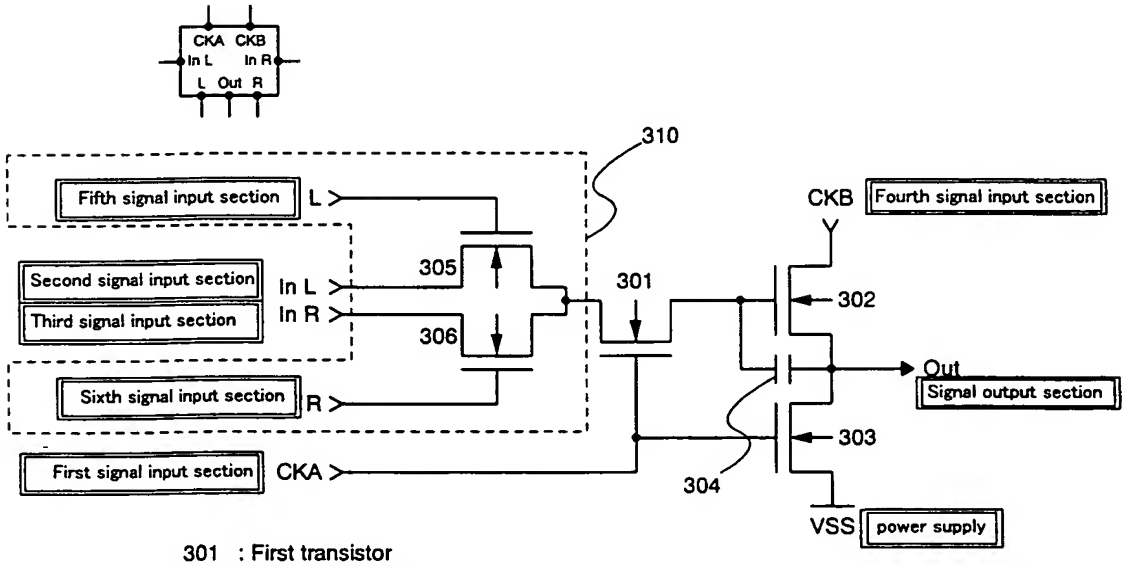
Fig. 2

Fig. 3A



CK1 : First clock signal
CK2 : Second clock signal
CK3 : Third clock signal
CK4 : Fourth clock signal
SP : Start pulse
LR : Input change signal
RL : Inverted input change signal

Fig. 3B



301 : First transistor
302 : Second transistor
303 : Third transistor
304 : Capacitor
305 : Fourth transistor
306 : Fifth transistor
310 : Input change circuit

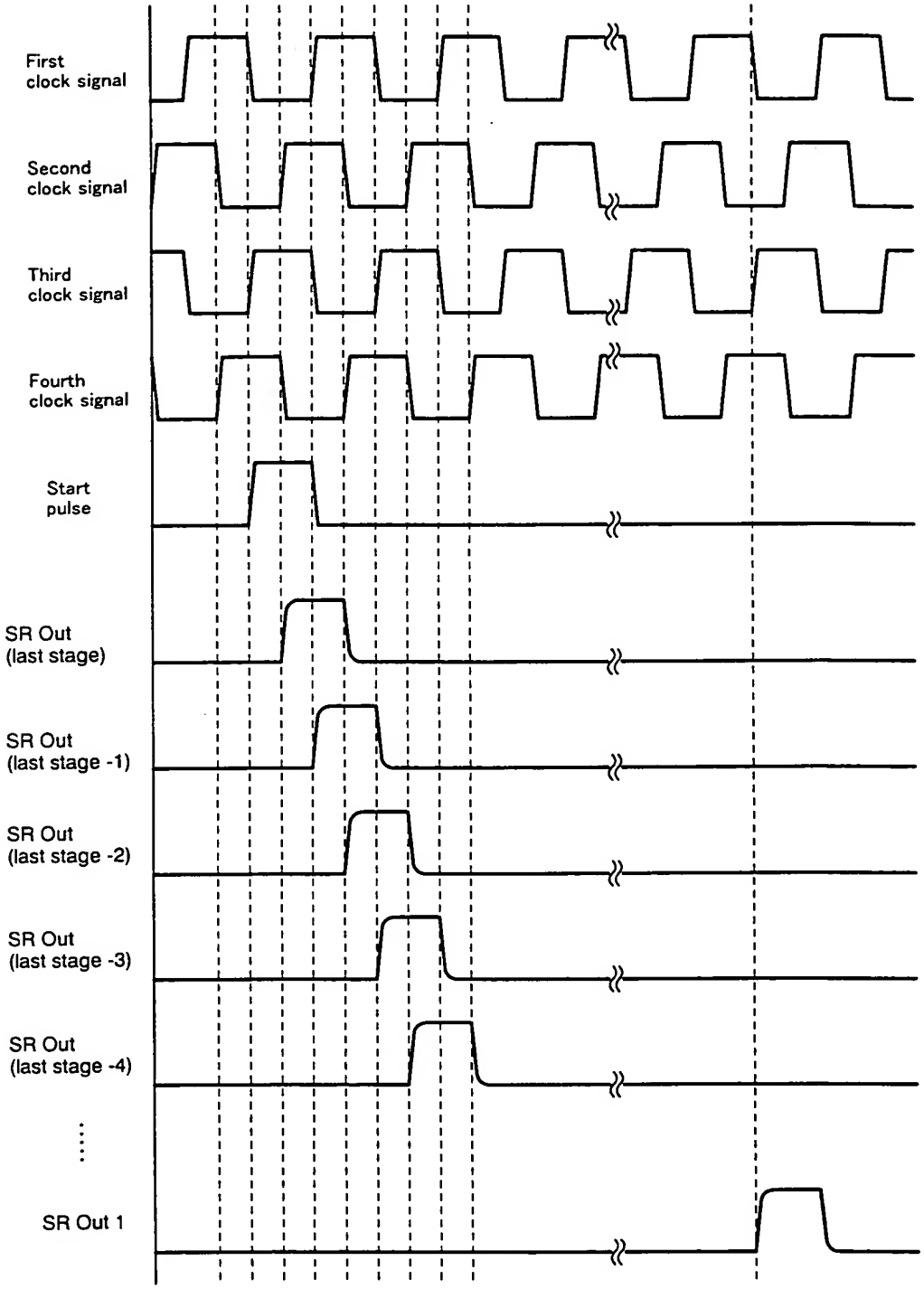

First clock signal
Second clock signal
Third clock signal
Fourth clock signal
Start pulse
SR Out (last stage)
SR Out (last stage -1)
SR Out (last stage -2)
SR Out (last stage -3)
SR Out (last stage -4)
SR Out 1

Fig. 4

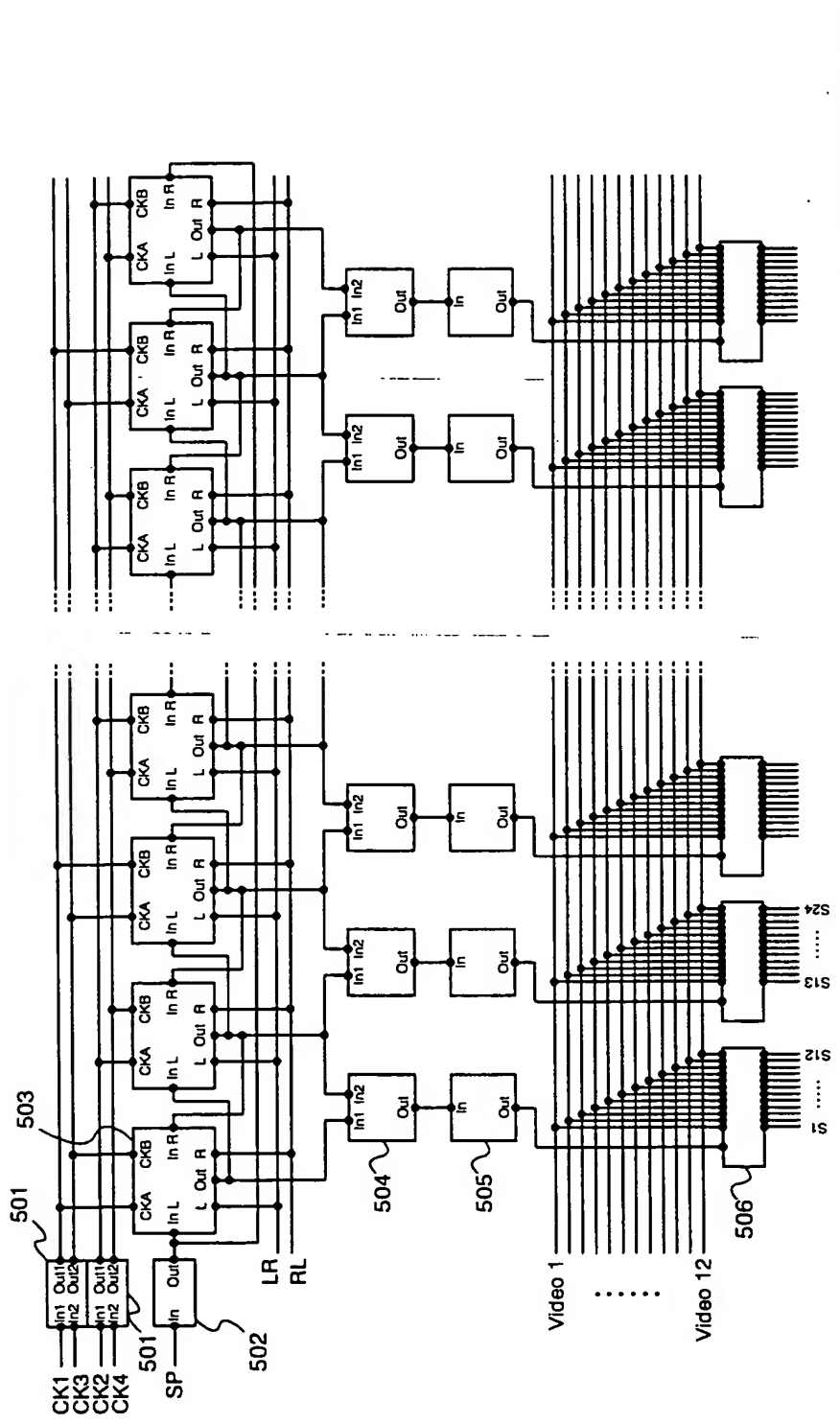

501 : Clock signal level shifter
502 : Start pulse level shifter
503 : pulse output circuit
504 : NAND circuit
505 : Buffer
506 : Sampling switch
CK1
CK3
CK2
CK4
SP
LR
RL
Video 1
Video 12
S1
S12
S13
S24

Fig. 5

Fig. 6A

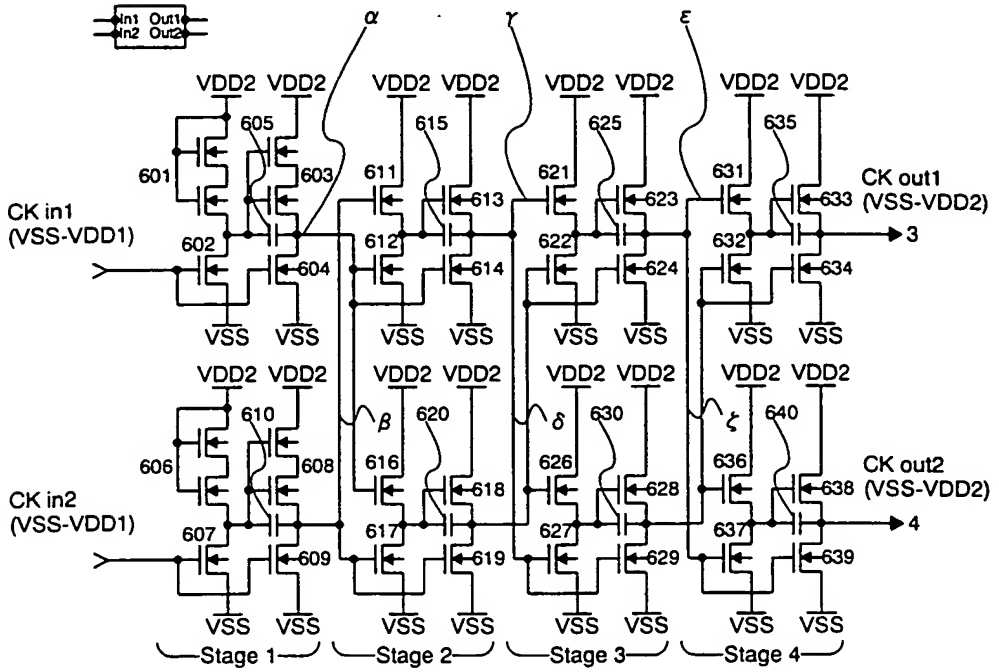


Fig. 6B

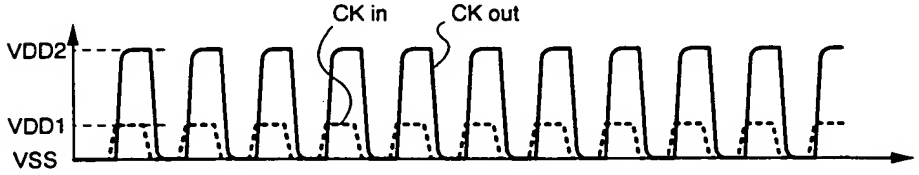
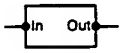


Fig. 6C 

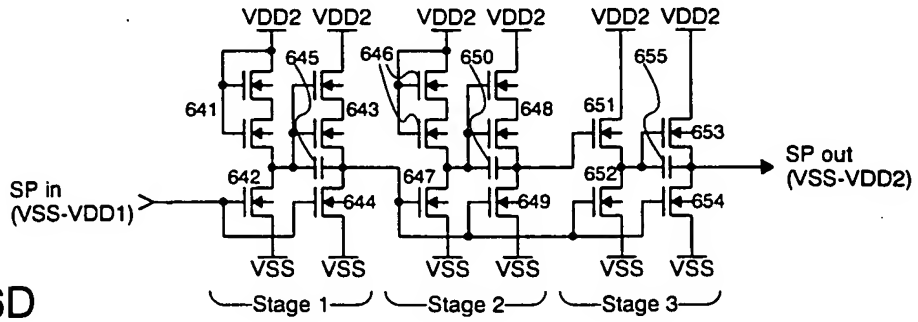


Fig. 6D

Fig. 7A

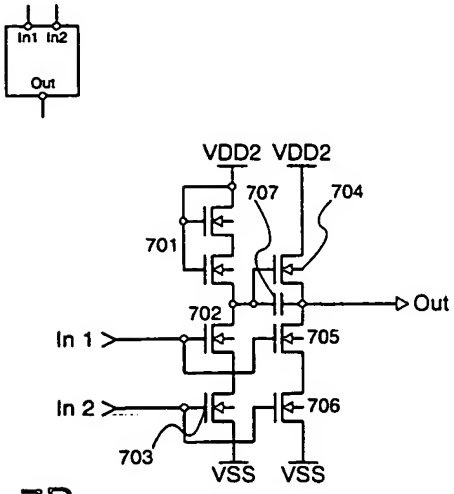


Fig. 7B

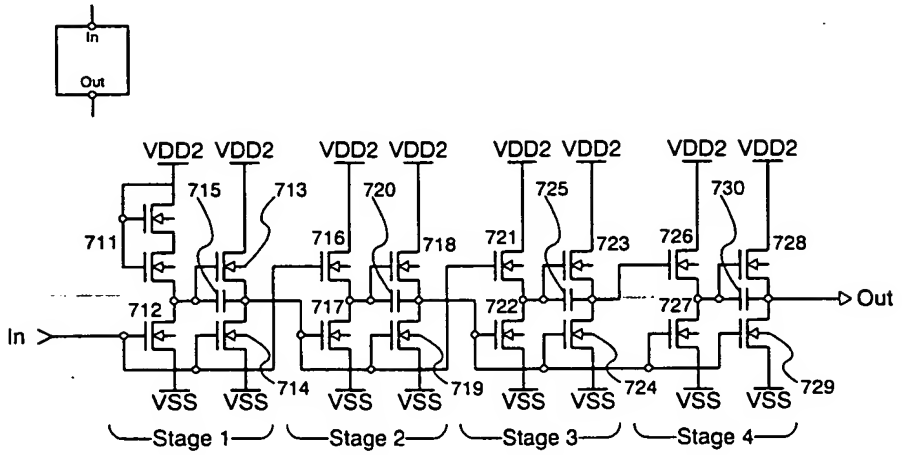
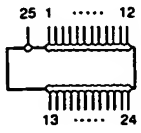
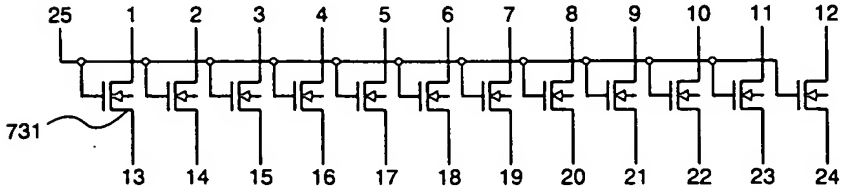


Fig. 7C





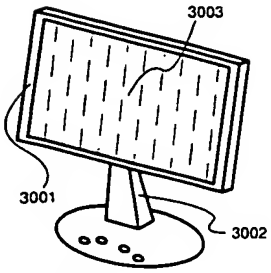


Fig. 8A

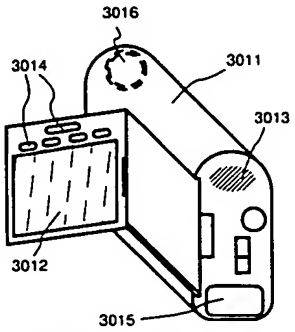


Fig. 8B

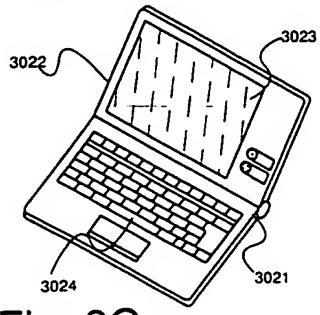


Fig. 8C

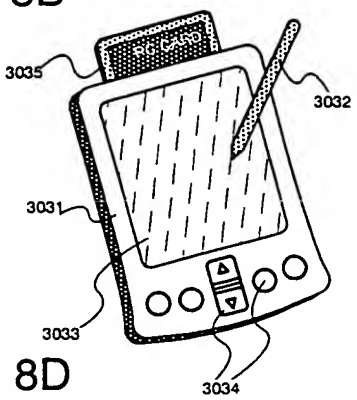


Fig. 8D

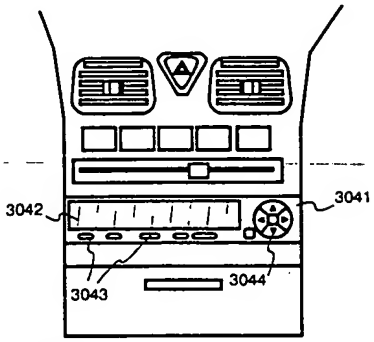


Fig. 8E

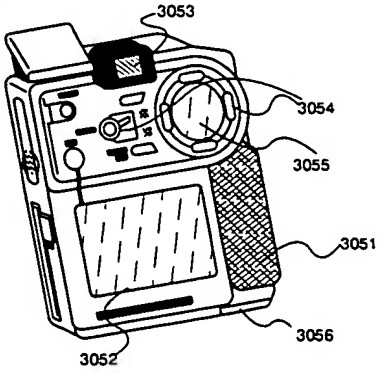


Fig. 8F

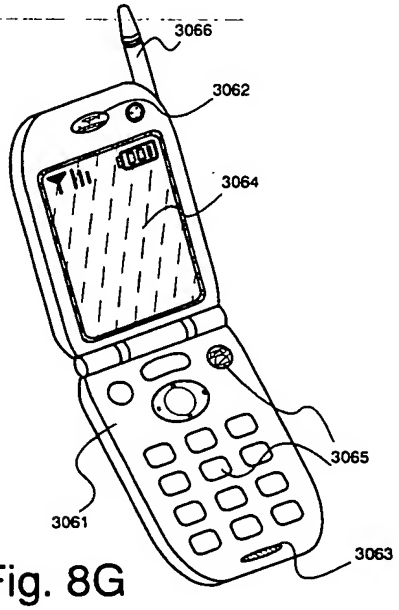


Fig. 8G

Fig. 9A

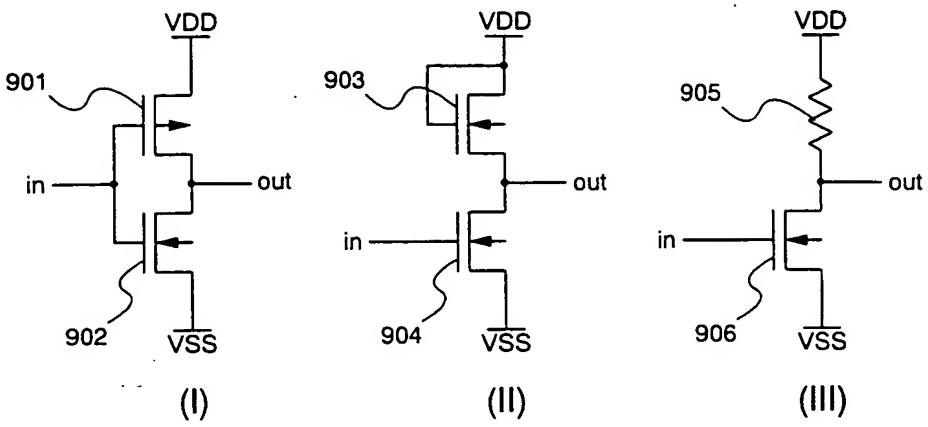


Fig. 9B

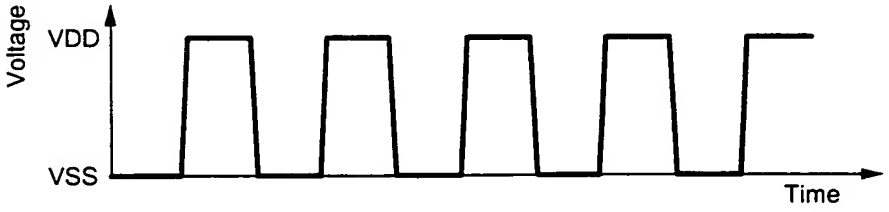


Fig. 9C

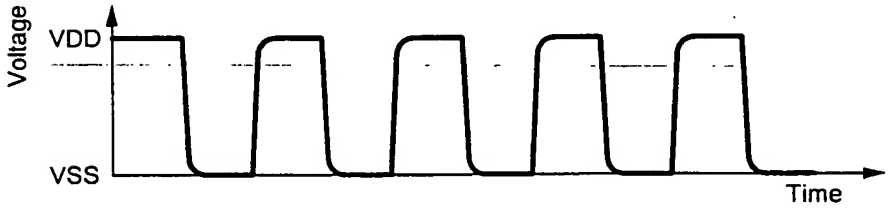


Fig. 9D

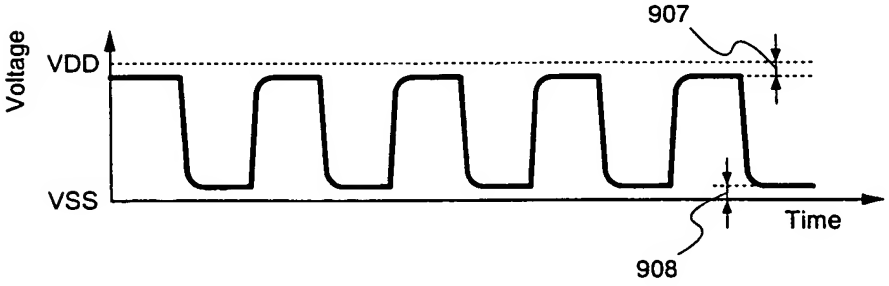
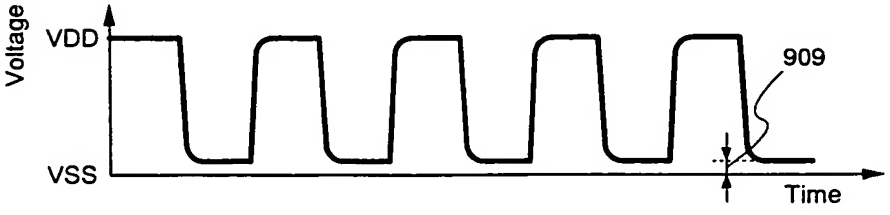


Fig. 9E



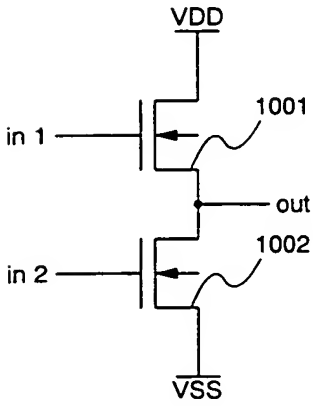


Fig. 10A

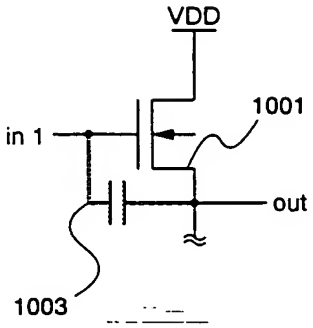


Fig. 10B

Fig. 11A

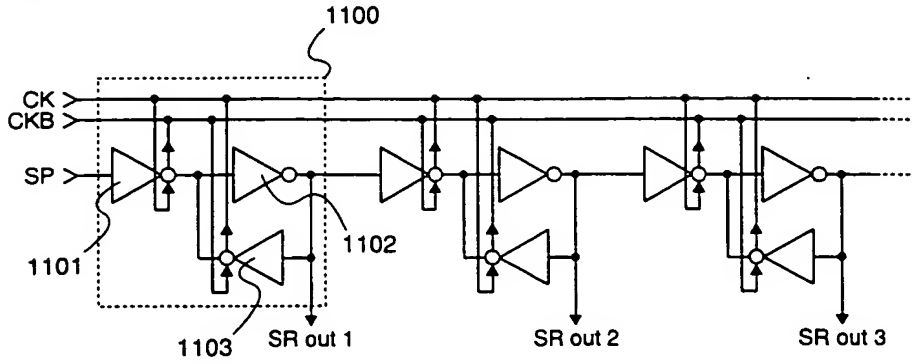


Fig. 11B

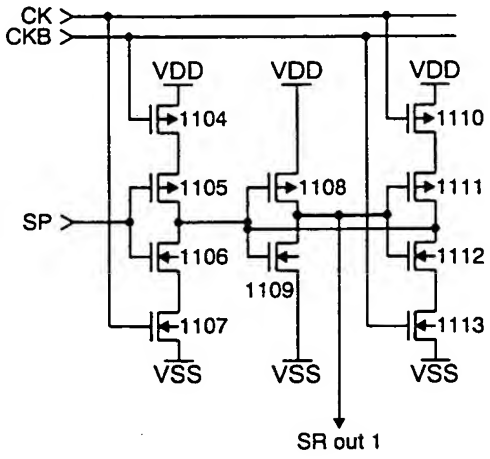
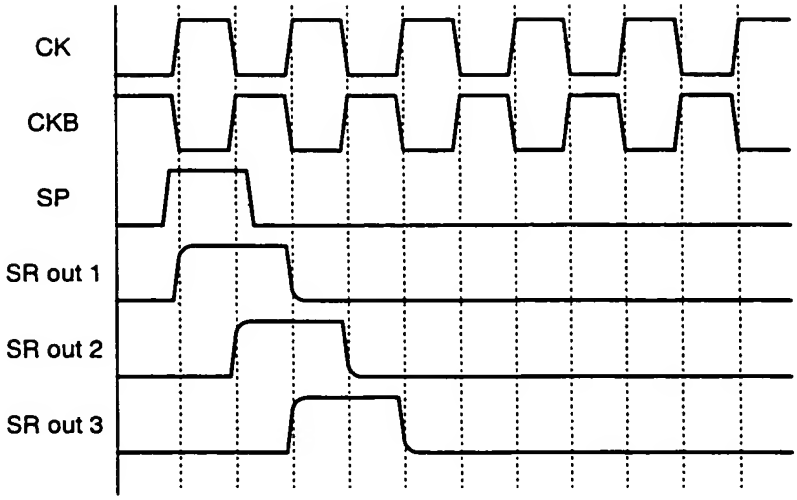


Fig. 11C



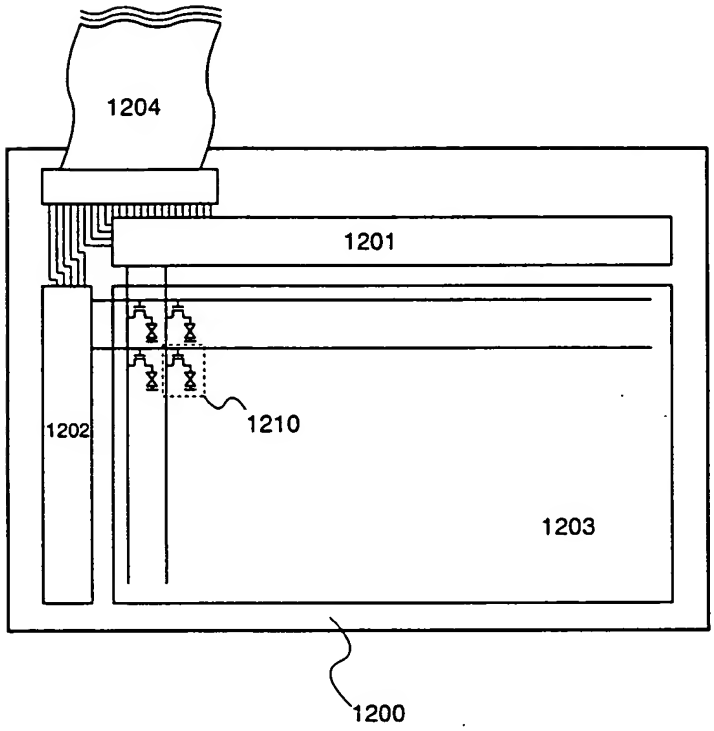
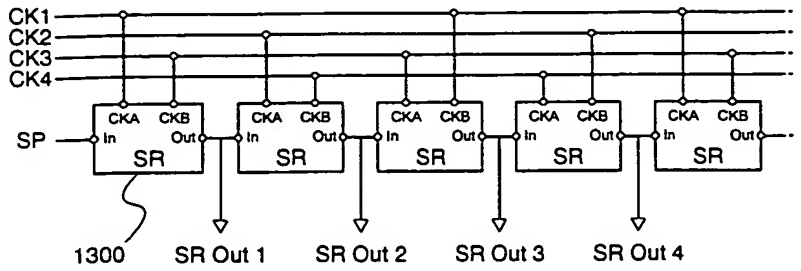


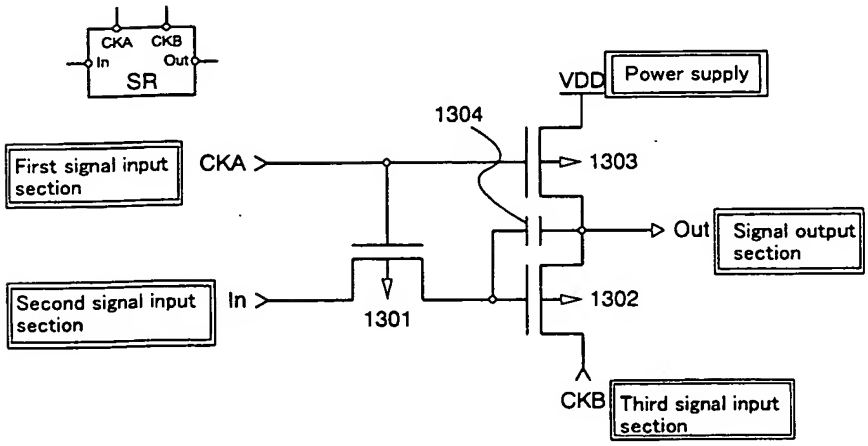
Fig. 12

Fig. 13A



CK1 : First clock signal
CK2 : Second clock signal
CK3 : Third clock signal
CK4 : Fourth clock signal
SP : Start pulse

Fig. 13B



1301 : First transistor
1302 : Second transistor
1303 : Third transistor
1304 : Capacitor

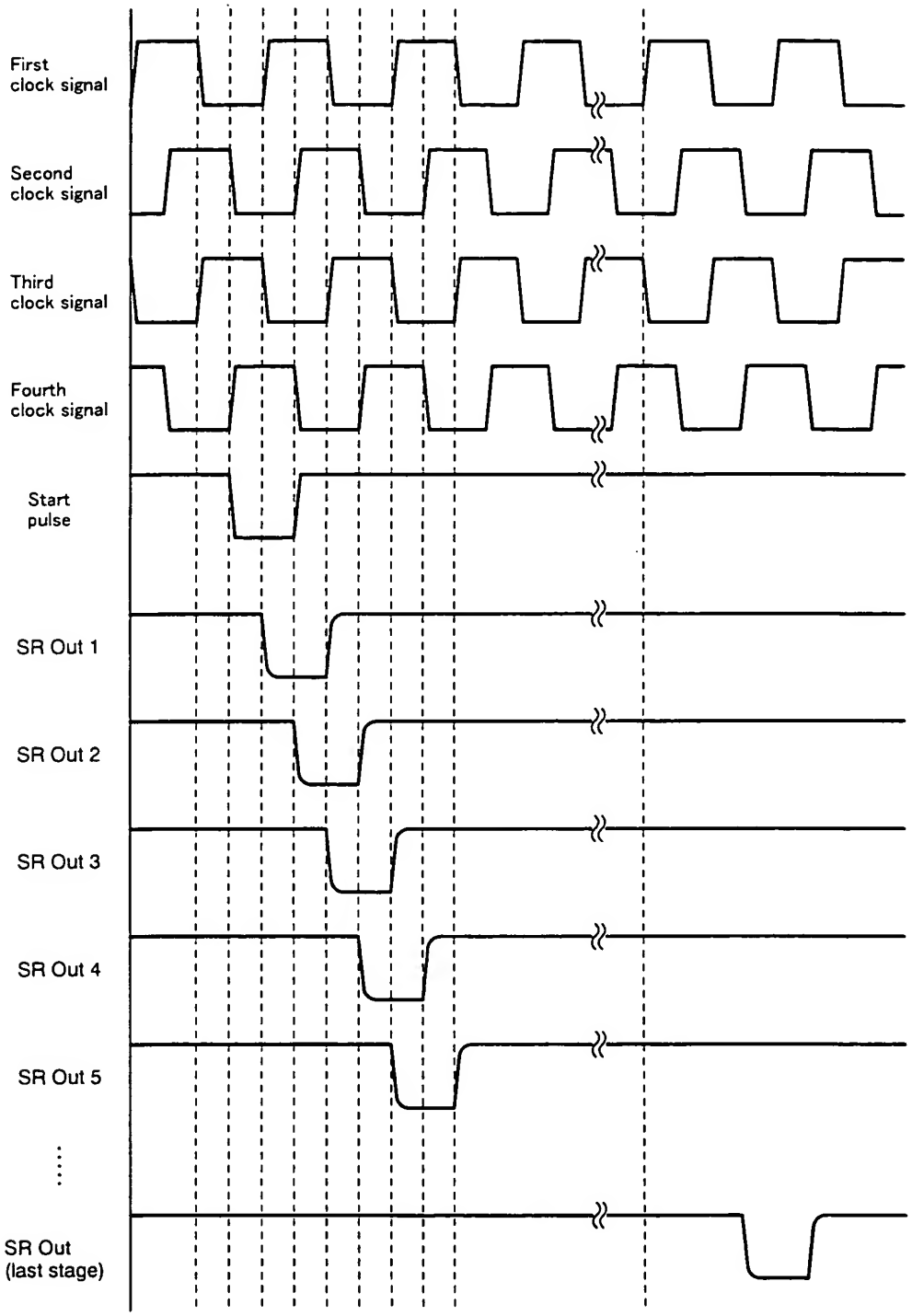

First clock signal
Second clock signal
Third clock signal
Fourth clock signal
Start pulse
SR Out 1
SR Out 2
SR Out 3
SR Out 4
SR Out 5
SR Out (last stage)

Fig. 14

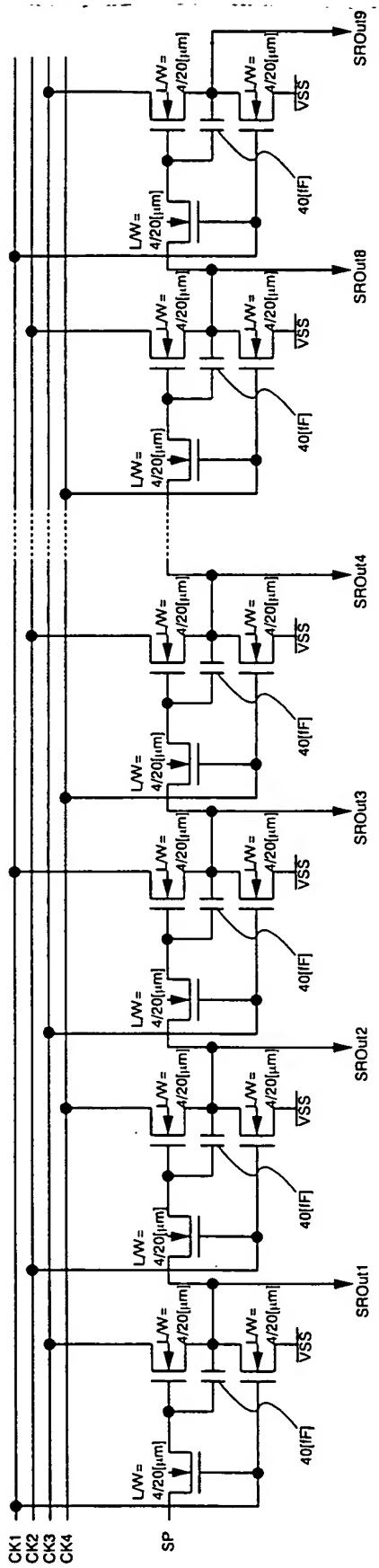

CK1
CK2
CK3
CK4
SP
SROut1
SROut2
SROut3
SROut4
SROut8
SROut9
VSS
L/W=
4/20[μm]
40[IF]

Fig. 15

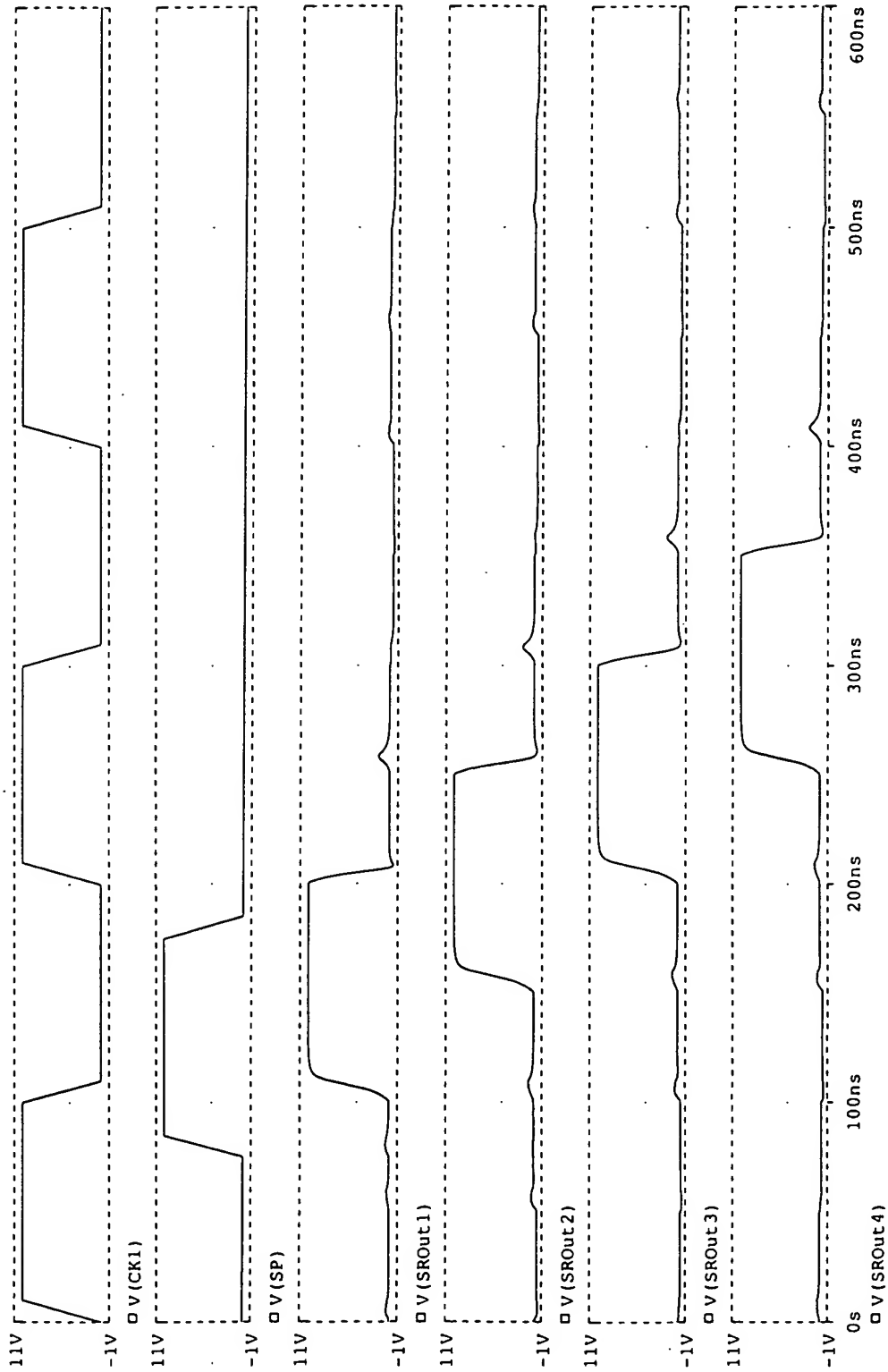

11V
-1V
V(CK1)
V(SP)
V(SROut1)
V(SROut2)
V(SROut3)
V(SROut4)
0s
100ns
200ns
300ns
400ns
500ns
600ns
Time

Fig. 16

Fig. 17A

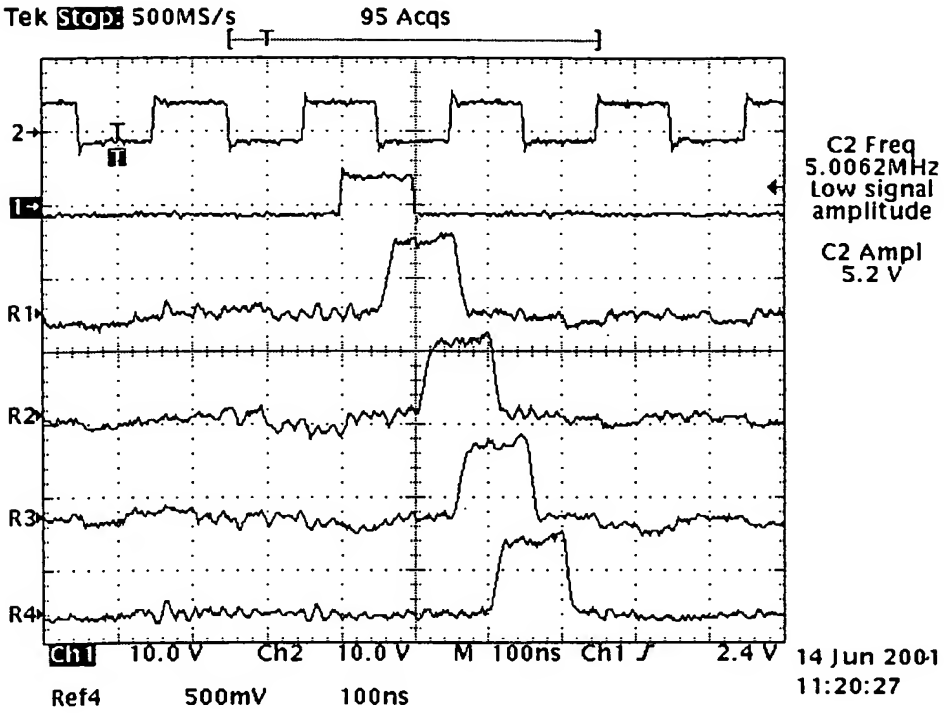


Fig. 17B